REMARKS

The present communication responds to the Office Action dated August 24, 2004, in the above-identified application. Claims 1-12 were pending in the application at the time the present Office Action was mailed. By this response, claims 1-2, 4, 7-8, and 10-12 are amended to improve readability or more precisely claim the applicant's technology; claims 3, 5-6, 9, and 11 are cancelled; and claims 13-20 are added. Accordingly, claims 1-2, 4, 7-8, and 10-20 are pending in the present application.

Claims 1-2 and 4-12 were rejected in the Office Action as unpatentable under 35 U.S.C. § 102(b) over U.S. Patent No. 6,038,867 ("Ho"). Claim 3 was rejected in the Office Action under 35 U.S.C. § 103(a) over Ho in view of U.S. Patent No. 6,327,688 ("Stolitzka").

The applicant's technology is directed to diagnostic testing of computer hardware and, more particularly, techniques for testing data path integrity within the hardware. The applicant's technology enables testing of system busses, data initiators (sources of data), and data targets (recipients of that data). The applicant's technology is further designed to operate in an open network, where components of the network may not provide specific hardware support for checking data.

In an aspect of the applicant's technology, the computer system (e.g., data storage router) may have at least two internal data paths between a processor and a memory controller. (See, e.g., Figure 2 of the application.) As an example, the processor and the memory controller may be physically coupled and further have a connection via a PCI bus to which the processor and the memory controller are separately coupled. Alternatively, the processor may be coupled to two separate PCI busses, and each PCI bus may be coupled to the memory controller. By thus having two internal data paths, the processor can write to or read from memory (via the memory controller) by transmitting or receiving data across the two data paths separately.

As an example, the processor 202 of Figure 2 may send a data test pattern using one data path (PCI bus 214a) and verify that the data was written correctly using the second path (PCI bus 214b). In this way, the processor may determine whether an I/O controller (210a, 210b, 220a, or 220b) is malfunctioning by writing a data test pattern to a region of memory 206, requesting the I/O controller to read the data test pattern from the memory and re-write the data test pattern to another region of the memory, and then comparing the contents of the two regions of memory to verify that the contents are identical. Because the writing and the reading/re-writing may be performed using physically separate data paths, malfunctioning components internal to the system 200 may be isolated. Further embodiments of the invention are described or illustrated in the applicant's specification and figures. Because the applicant's technology detects various hardware failures, it enables end-to-end data path verification.

Ho is directed to a loop-back test apparatus for SCSI interfaces. (Ho, Abstract.) Ho's technique enables a host computer to test a SCSI controller by performing a loop-back test without requiring use of a target device coupled to the SCSI controller. (Ho, 2:5-11, 2:20-24, and 6:105.) In conventional systems, when a host sends data to a target and then retrieves the data to determine whether the data was received by the target correctly, the host may be unable to determine which component in the data path between the host and the target caused an error. For example, the SCSI controller or the target may have caused an error because of a malfunction. Using Ho's technique, the host is able to determine whether the SCSI controller caused the error by requesting the SCSI controller to perform a loop-back test that does not require the use of a target. Furthermore, one skilled in the art would recognize that a SCSI bus has a single, shared bidirectional data path in which direction is determined by an IO signal. Ho makes clear that his technique uses such a bidirectional bus. (See Ho, 5:2-3 and 5:61-64.)

Stolitzka is directed to data integrity verification of a data communication system between two devices. More specifically, in Stolitzka, a bus device that receives a

message always responds by sending a check sequence back to a device that originated the message. (Stolitzka, Abstract.)

Neither Ho nor Stolitzka teach or suggest having more than one physical data path to test aspects of a computer system (e.g., data storage router). By having multiple physical data paths, the applicant's technology is able to determine which component(s) in a data path may be malfunctioning. Furthermore, neither Ho nor Stolitzka enable end-to-end data path verification. For example, in neither Ho's technique nor Stolitzka's technique would it be possible to determine that a particular bus itself is malfunctioning because data is transmitted and verified using the same bus.

The applied references do not recite the feature of having multiple physical data paths over which to perform a single test, and so the applicant respectfully submits that claims reciting this feature are allowable over the applied references. Independent claim 1 has been amended to clarify that the computer system has at least two physical data paths over which a single test is performed, and so is allowable over the applied references. Claims 2, 4, 7-8, and 10-12 are dependent on claim 1 and thus are allowable for similar reasons. Newly added claims 13-20 also recite a feature of having at least two physical data paths for performing a test. These claims are also allowable for similar reasons.

Claims 7 and 8 were objected to in the Office Action as being of improper dependent form. The applicant respectfully submits that the amendment to these claims overcome this objection.

The first full paragraph appearing on page 6 of the applicant's specification as originally filed is moved to page 12 by this response. The paragraph was inadvertently placed in the background section. The paragraph, as moved, is substantially identical to the paragraph as originally filed. No new matter is added by the move.

The second full paragraph of page 5 of the applicant's specification as originally filed is amended to correct typographical errors and improve readability.

Conclusion

In view of the foregoing, the claims pending in the application comply with the requirements of 35 U.S.C. § 112 and patentably define over the applied art. A Notice of Allowance is, therefore, respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-6478.

Respectfully submitted,
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